

3-Vrms Cap-Less Line Driver with Adjustable Gain

Features

- Operation Voltage: 3V to 5.5V
- Cap-less Output
 - Eliminates Output Capacitors
 - Improves Low Frequency Response
 - Reduces POP/Clicks
- Low Noise and THD
 - SNR > 102dB
 - Typical $V_n < 12\mu\text{Vrms}$
 - THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
 - 2Vrms at 3.3V Supply Voltage
 - 3Vrms at 5V Supply Voltage
- single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time : 0.5ms
- Integrated De-Pop Control
- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

Ordering Information

Applications

- LCD / PDP TVs
- CD / DVD players
- Set-Top Boxes
- Home Theater in Box

Description

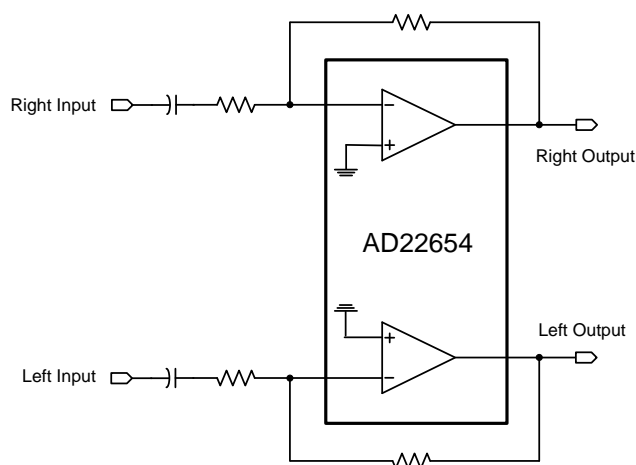
The AD22654 is a 3-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22654 is capable of delivering 3-Vrms output into a 2.5k Ω load with 5V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22654 is Build-in shutdown control and de-pop control sequence also help AD22654 to be a pop-less device.

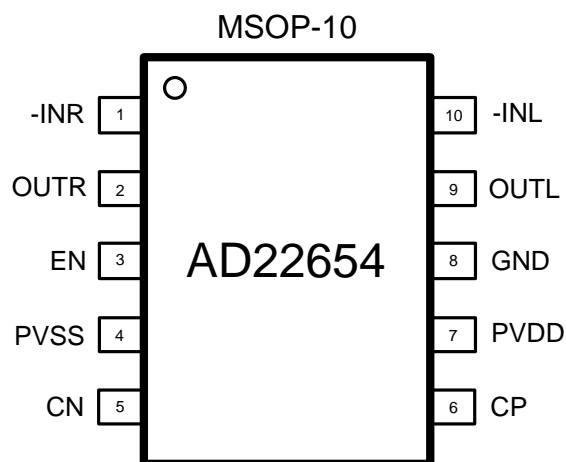
The AD22654 is available in a 10-pin MSOP package.

Product ID	Package	Packing	Comments
AD22654-MH10NAT	MSOP-10	80 Units / Tube 100 Tubes / Small Box	Green(HF)
AD22654-MH10NAR		3k Units Tape & Reel	

Simplified Application Circuit



Pin Assignments

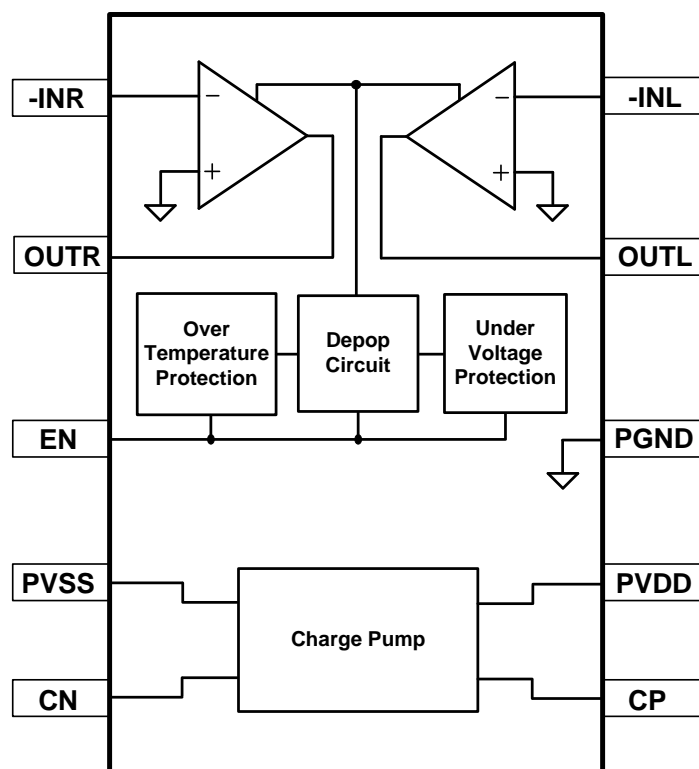


Pin Description

No.	Name	Type ⁽¹⁾	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

(1) I=input, O=output, P=power

Functional Block Diagram



Available Package

Package Type	Device No.	θ_{ja} ($^{\circ}\text{C}/\text{W}$) ⁽¹⁾	θ_{jc} ($^{\circ}\text{C}/\text{W}$) ⁽²⁾
MSOP-10	AD22654	120	45

(1) θ_{ja} is measured at room temperature ($T_A=25^{\circ}\text{C}$), natural convection environment test board, which is constructed with a thermal efficient, 2-layers PCB. The measurement is tested using the JEDEC51-3 thermal measurement standard.

(2) θ_{jc} represents the heat resistance for the heat flow between the chip and package's top surface.

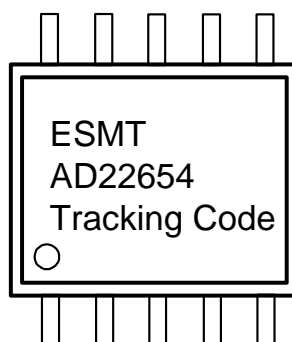
Marking Information

AD22654

Line 1 : LOGO

Line 2 : Product No.

Line 3 : Tracking Code



Absolute Maximum Ratings ⁽¹⁾

SYMBOL	PARAMETER	VALUE	UNIT
	Supply Voltage, V_{DD} to GND	-0.3 to 6.0	V
V_I	Input Voltage	VSS -0.3 to VDD+0.3	V
R_L	Minimum load impedance	> 600	Ω
	EN to GND	-0.3 to VDD+0.3	V
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$
T_J	Maximum operating junction temperature range	-40 to 150	$^{\circ}\text{C}$

(1) The absolute maximum ratings are limiting values of operation, safety of the device cannot be guaranteed if beyond those values.

Recommended Operating Conditions

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0		5.5	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	$^{\circ}\text{C}$
R_L	Load Resistance		600			Ω

Electrical Characteristics

PVDD=3.3V, $T_A=25^{\circ}\text{C}$, $R_L=2.5\text{k}\Omega$, $C_{FLY}=C_{PVSS}=1\mu\text{F}$, $C_{IN}=1\mu\text{F}$, $R_I=10\text{k}\Omega$, $R_F=20\text{k}\Omega$ (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	Min	NOM	Max	UNIT
I_{DD}	V_{DD} Supply Current	EN= V_{DD}		7	15	mA
I_{SD}	V_{DD} Shutdown Current	EN=0V, $V_{DD}=5.5\text{V}$			5	μA
II	Input Current	EN pin		0.1		μA
V_O	Output Voltage (Outputs In Phase)	THD+N=1%, $V_{DD}=3.3\text{V}$, $f_{IN}=1\text{kHz}$		2.2		Vrms
		THD+N=1%, $V_{DD}=5\text{V}$, $f_{IN}=1\text{kHz}$		3.4		
		THD+N=1%, $V_{DD}=5\text{V}$, $f_{IN}=1\text{kHz}$, $R_L=100\text{k}$		3.5		
THD+N	Total Harmonic Distortion Plus Noise	$V_O=2\text{Vrms}$, $f_{IN}=1\text{kHz}$		0.002		%
Crosstalk	Channel Separation	$V_O=2\text{Vrms}$, $f_{IN}=1\text{kHz}$		-110		dB
V_N	Output Noise	$R_I=10\text{k}$, $R_F=10\text{k}$		11	15	μVrms

Electrical Characteristics (Con't)

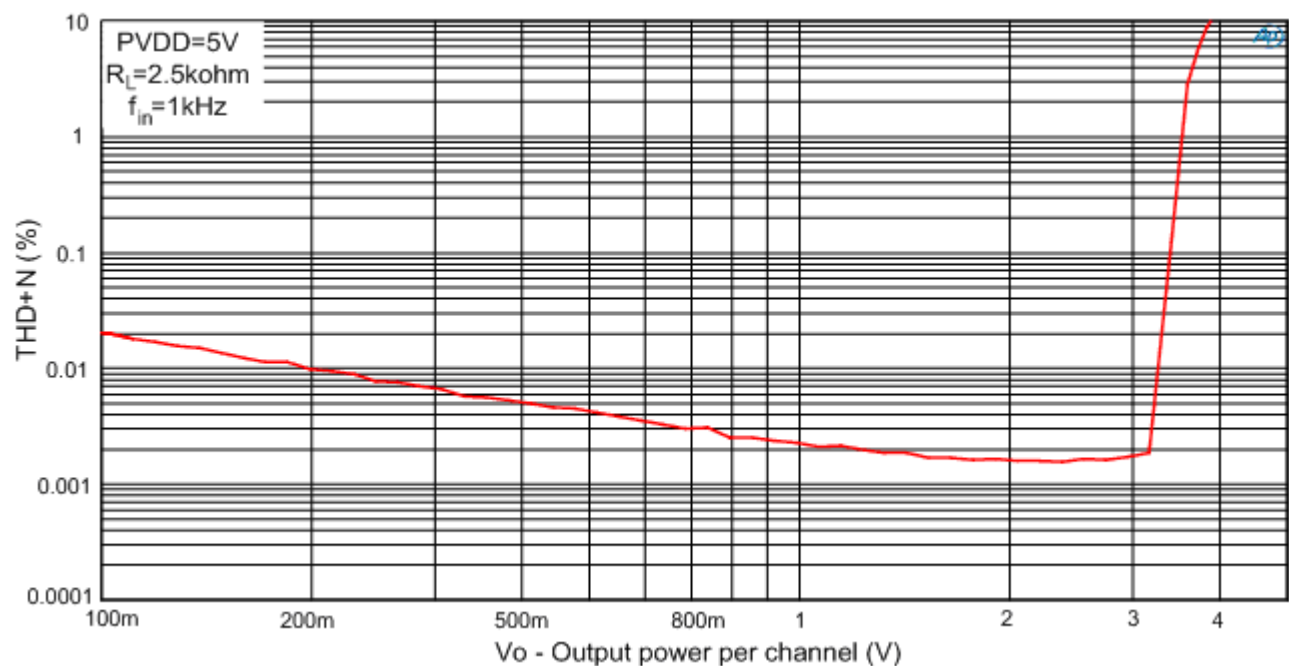
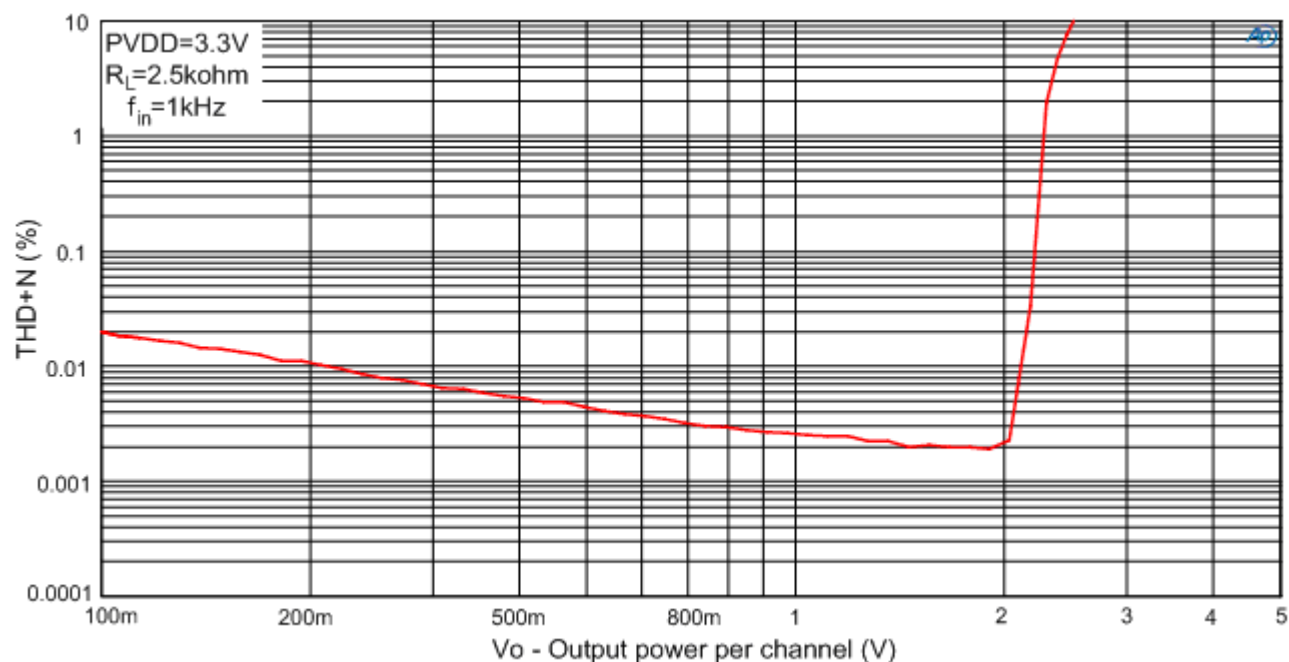
PVDD=3.3V, T_A=25°C, R_L=2.5kΩ, C_{FLY}=C_{PVSS}=1μF, C_{IN}=1μF, R_I=10kΩ, R_F=20kΩ (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	Min	NOM	Max	UNIT
V _{SR}	Slew Rate			8		V/μs
SNR	Signal to Noise Ratio	V _O =2Vrms, R _I =10k, R _F =10k, A-weighted		107		dB
G _{BW}	Unit-Gain Bandwidth			8		MHz
A _{VO}	Open-Loop Gain		80			dB
V _{OS}	Output Offset Voltage	V _{DD} =3V to 5.5V, Input Grounded	-5		5	mV
PSRR	Power Supply Rejection Ratio	V _{DD} =3V to 5.5V, V _{rr} =200mVrms, f _{IN} =1kHz		-80	-60	dB
R _I	Input Resistor Range		1	10	47	kΩ
R _F	Feedback Resistor Range		4.7	20	100	kΩ
f _{CP}	Charge-Pump Frequency		400	500	600	kHz
	Maximum capacitive Load			220		pF
TSD	Over Temperature Protection Level			150		°C
T _{start-up}	Start-up Time			0.5		ms

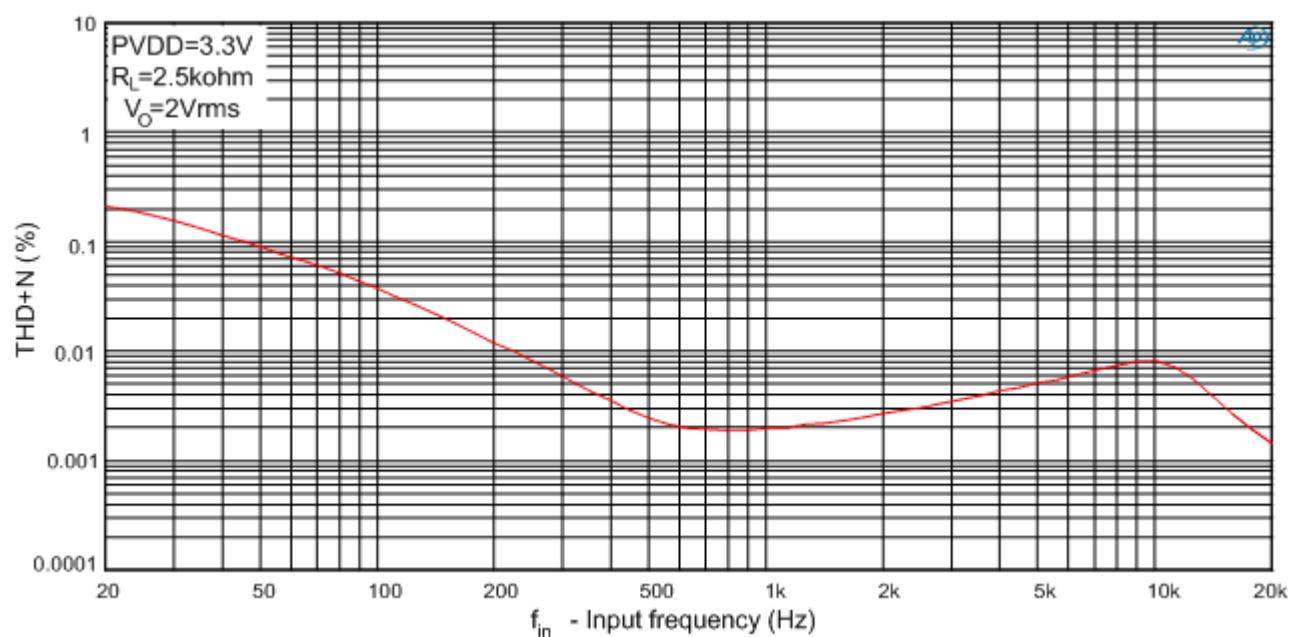
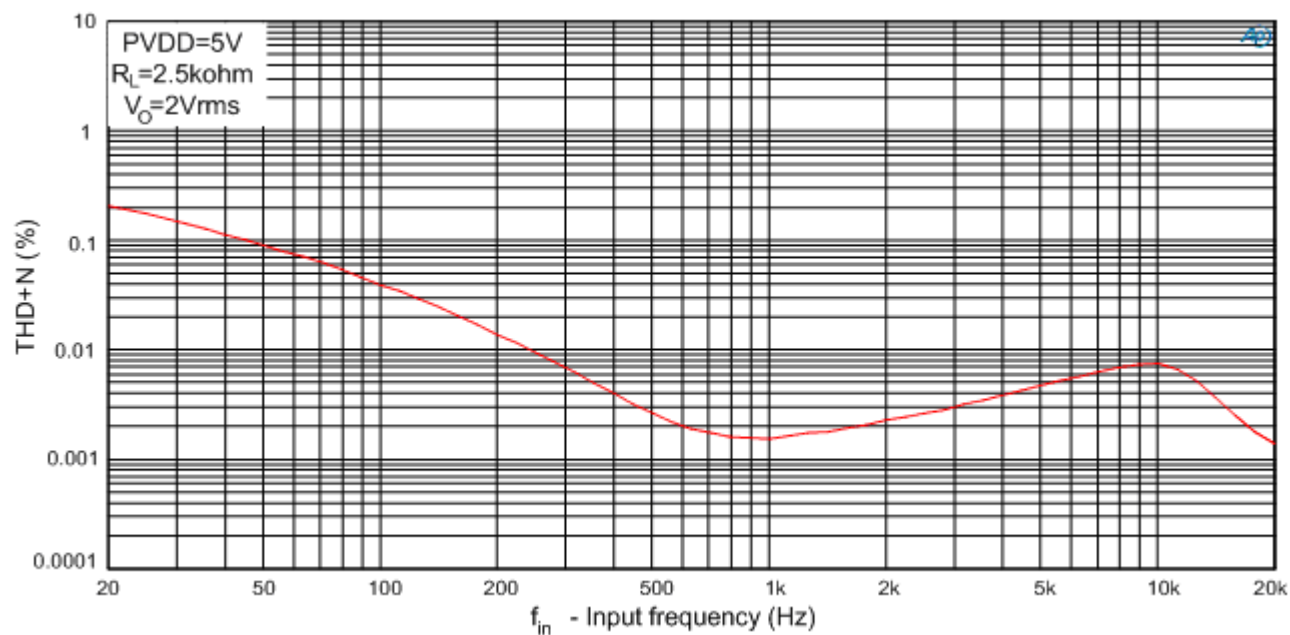
Typical Characteristics

PVDD=3.3V, $T_A=25^\circ\text{C}$, $R_L=2.5\text{k}\Omega$, $C_{FLY}=C_{PVSS}=1\mu\text{F}$, $C_{IN}=1\mu\text{F}$, $R_I=10\text{k}\Omega$, $R_F=20\text{k}\Omega$ (unless otherwise noted)

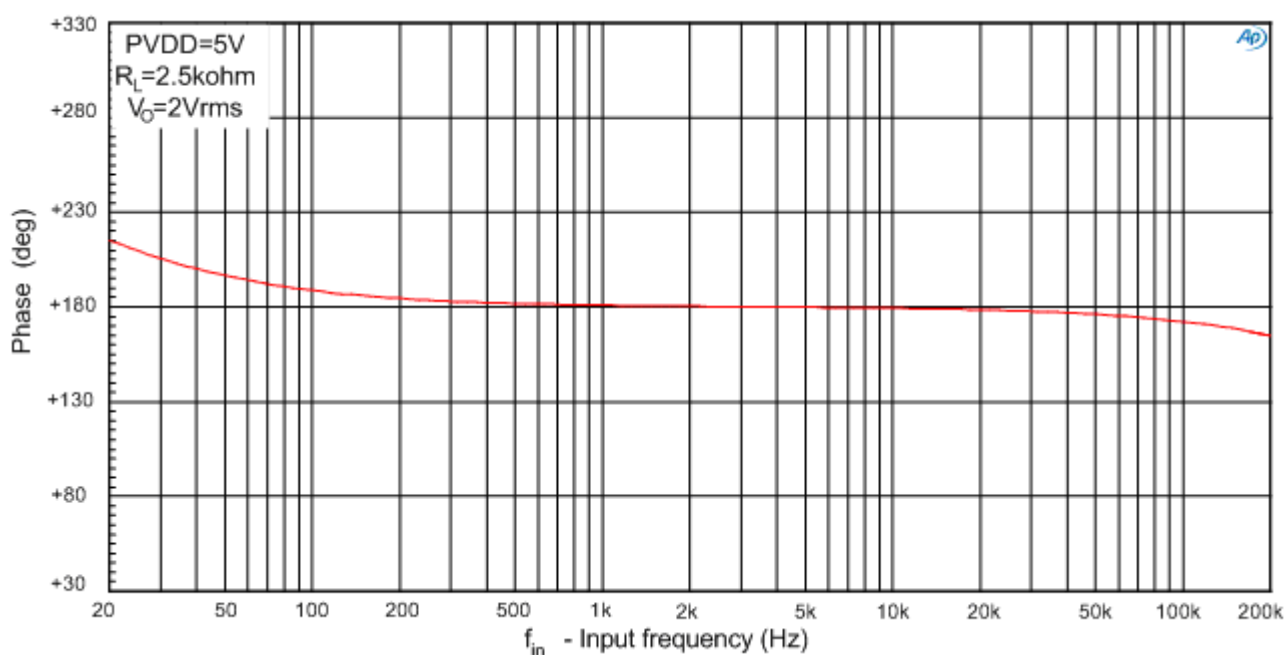
● Total Harmonic Distortion + Noise (THD+N) vs. Output Power



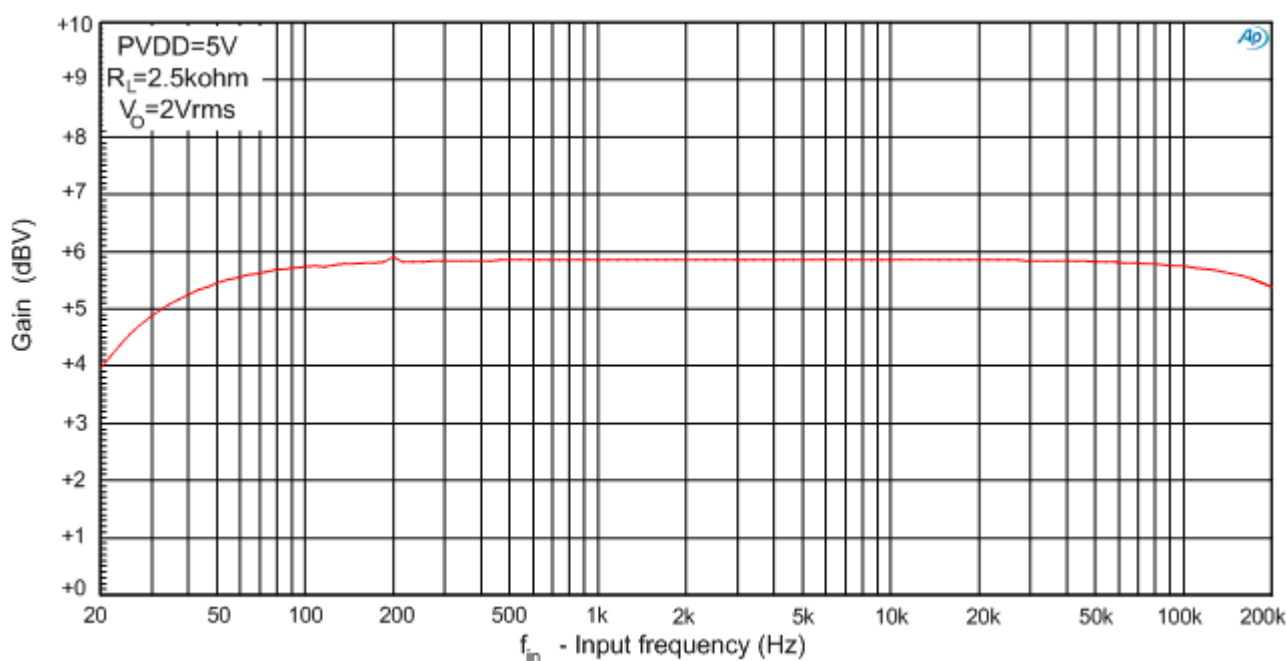
● Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency



● Phase vs. Signal Frequency



● Gain vs. Signal Frequency



Application Information

Line Driver Amplifiers Operation

A conventional inverting line-driver amplifier always requires an output dc-blocking capacitor and a bypass capacitor, see Figure 1. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge V_{OUT} from 0V to $V_{DD}/2$.

For a cap-less line driver, see figure 2, a negative supply voltage (-VDD) is produced by the integrated charge-pump, and feeds to line driver's negative supply instead of ground. The positive input can directly connect to ground without a C_{BYPASS} , and V_{OUT} is biased at ground which can eliminate the output dc-blocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.

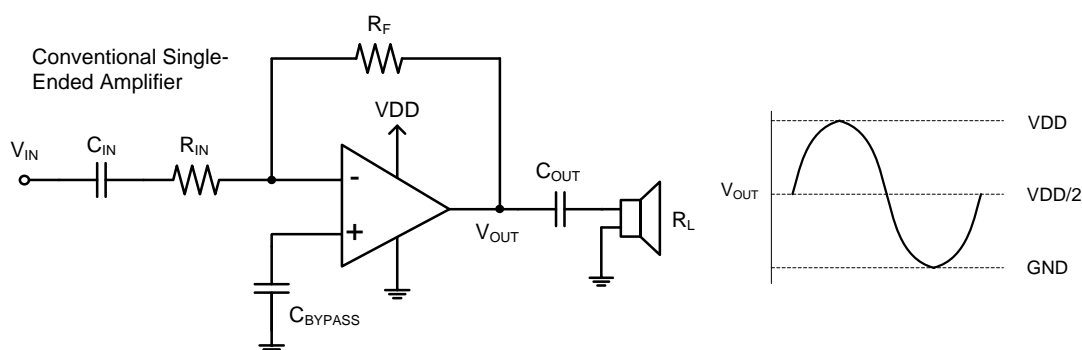


Figure 1. Conventional Line Driver Amplifier

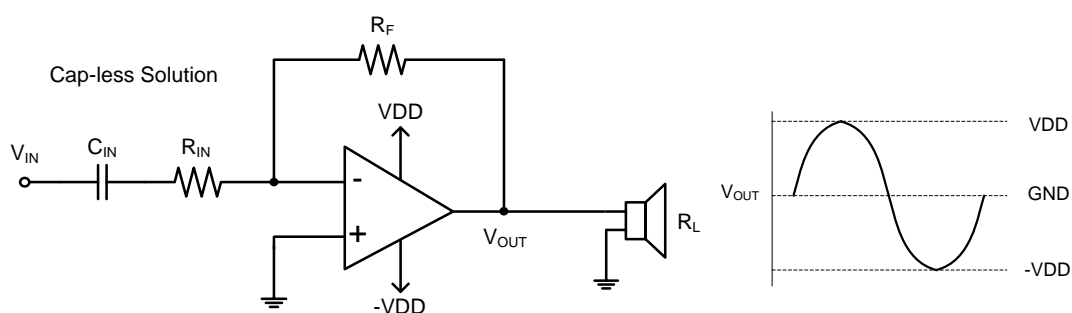


Figure 2. Cap-less Line Driver Amplifier

■ Charge-Pump Operation

The charge-pump is used to generate a negative supply voltage to supply to line-driver. It needs two external capacitors, C_{FLY} and C_{PVSS} , for normal operation, see figure 3 (a). The operation can be analyzed with two phase. In phase I, see figure 3 (b), C_{FLY} is charged to PVDD, and in phase II, see figure 3 (c), the charges on C_{FLY} are shared with C_{PVSS} , that makes PVSS a negative voltage. After an adequate clock cycles, PVSS will be equaled to $-PVDD$. Low ESR capacitors are recommended, and the typical value of C_{FLY} and C_{PVSS} is 1 μ F. A smaller capacitance can be used, but the maximum output voltage may be reduced.

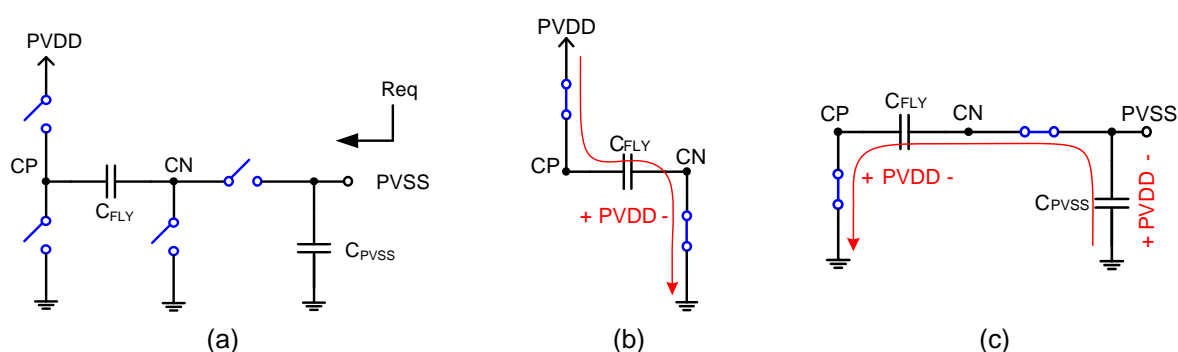


Figure 3. Charge-Pump Operation

■ Enable Function

The enable function is used to reduce power consumption while the device is not in use. When a logic low is applied to this pin, the overall circuits are turned off. Line driver output and PVSS are pulled to ground. When a logic high is applied to enable pin, the PVSS is started to build-up and line driver output signal is released after about 0.5ms typically.

■ Decoupling Capacitors

A low ESR power supply decoupling capacitor is required for better performance. The capacitor should place as close to chip as possible, the value is typically 1 μ F. For filtering low frequency noise signals, a 10 μ F or greater capacitor placed near the chip is recommended.

■ Input Blocking Capacitors (C_{IN})

An input blocking capacitor is required to block the dc voltage of the audio source and allows the input to bias at a proper dc level for optimum operation. The input capacitor and input resistor (R_I) form a high-pass filter with the corner frequency determined as following equation:

$$f_c = \frac{1}{2\pi R_I C_{IN}}$$

■ Gain Setting Resistors (R_I and R_F)

The line driver's gain is determined by R_I and R_F . The configuration of the amplifier is inverting type, see figure 4. The gain equation is listed as follows:

Inverting configuration:
$$A_v = -\frac{R_F}{R_I}$$

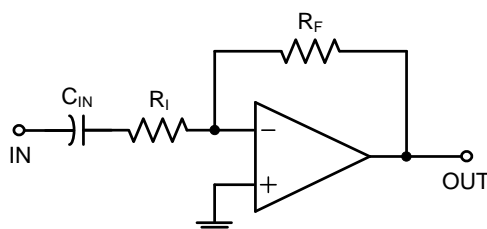


Figure 4. Line Driver Amplifier Configurations

The values of R_I and R_F must be chosen with consideration of stability, frequency response and noise. The recommended value of R_I is in the range from 1k Ω to 47k Ω , and R_F is from 4.7k Ω to 100k Ω for. The gain is in the range from -1V/V to -10V/V for inverting configuration. Table 1 lists the recommended resistor values for different configurations.

R_I (k Ω)	R_F (k Ω)	Inverting Input Gain (V/V)
22	22	-1
15	30	-2
33	68	-2.1
10	100	-10

Table 1. Recommended Resistor Values

■ Second-Order Filter Configuration

AD22654 can be used like a standard OPAMP. Several filter topologies can be implemented by using AD22654, single-ended input configuration, see figure 5. For inverting input configuration, the overall

gain is $-\frac{R2}{R1}$, the high-pass filter's cutoff frequency is $\frac{1}{2\pi R1C3}$, the low-pass filter's cutoff frequency

is $\frac{1}{2\pi\sqrt{R2R3C1C2}}$, The detail component values are listed on table 2.

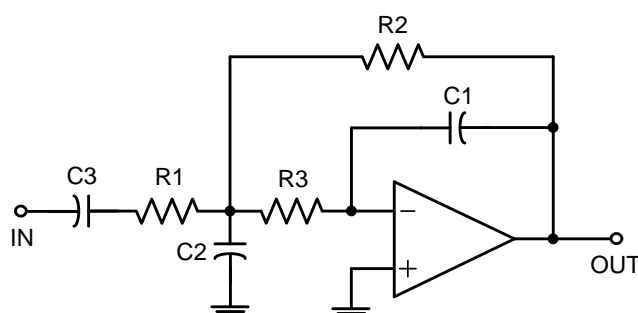


Figure 5. Second-order Active Low-Pass Filter

Gain (V/V)	High Pass (Hz)	Low Pass (kHz)	C1 (pF)	C2 (pF)	C3 (μF)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
-1	1.6	40	100	680	10	10	10	24
-1.5	1.3	40	68	680	15	8.2	12	30
-2	1.6	60	33	150	6.8	15	30	47
-2	1.6	30	47	470	6.8	15	30	43
-3.33	1.2	30	33	470	10	13	43	43
-10	1.5	30	22	1000	22	4.7	47	27

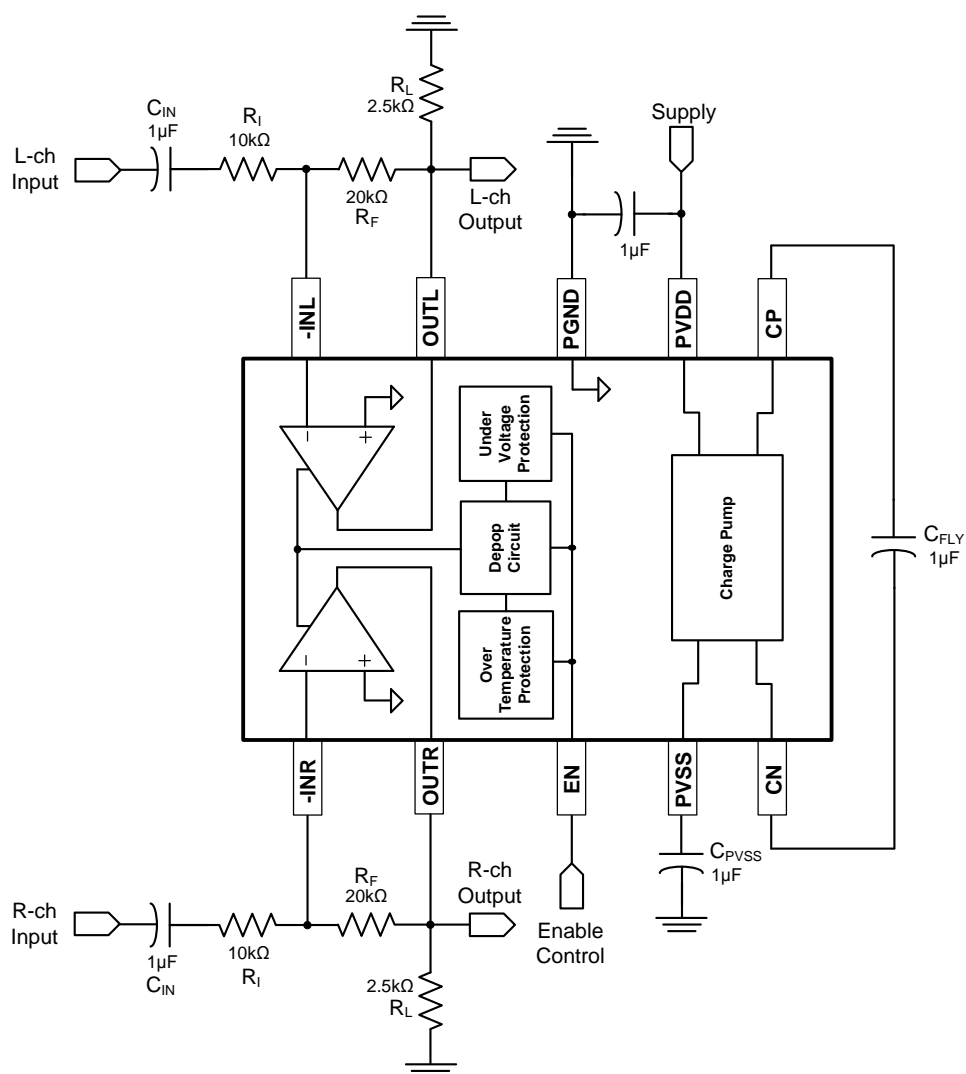
Table 2. Second-order Low-Pass Filter Specifications

■ Over-Temperature Protection

AD22654 provide an over-temperature protection to limit the junction temperature to 150°C. As junction temperature exceeds 150°C, internal thermal sensor will turn off the drivers immediately. The drivers will turn on again if the junction temperature is smaller than 130°C. A 20°C hysteresis is designed to lower the average junction temperature during continuous thermal overload conditions, increasing lifetime of the chip.

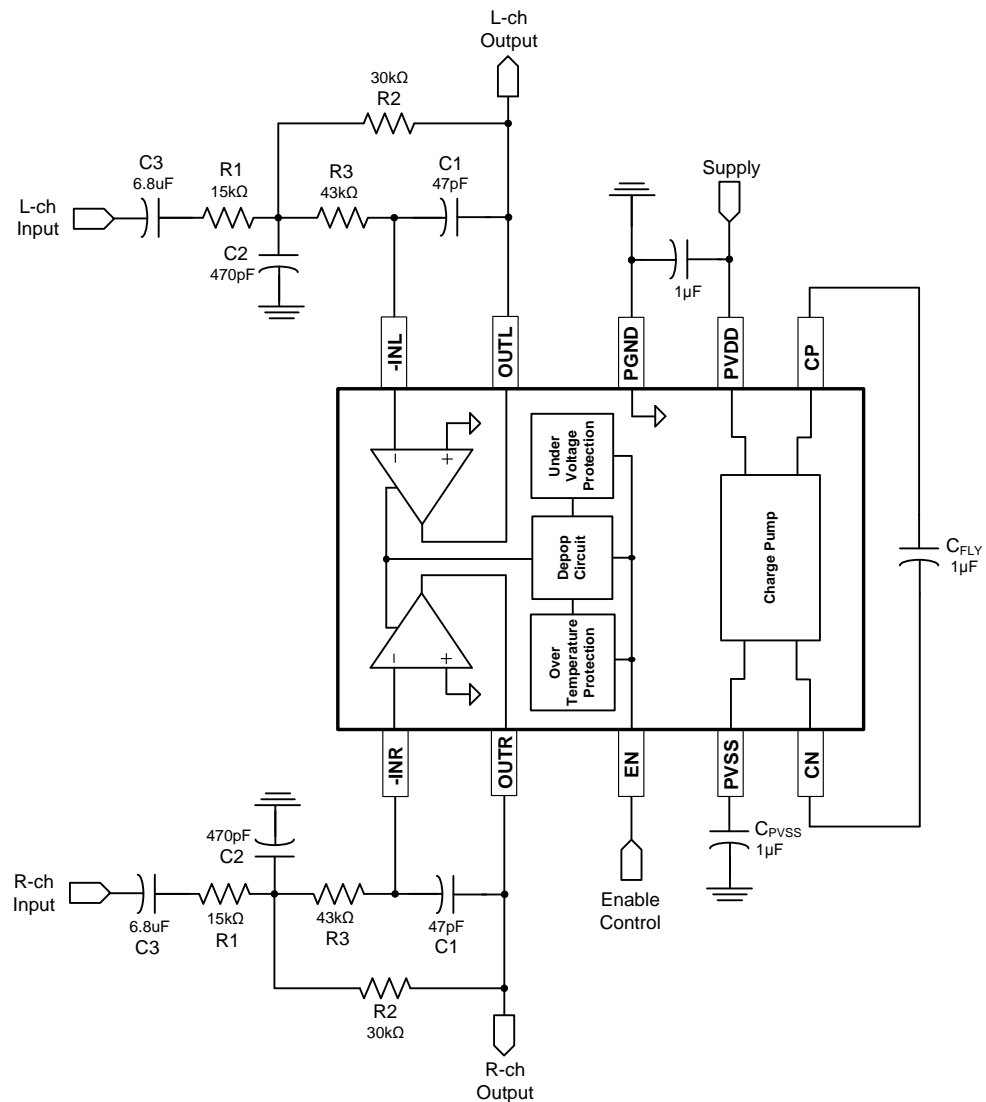
Typical Application Circuit

■ Line Driver Amplifier

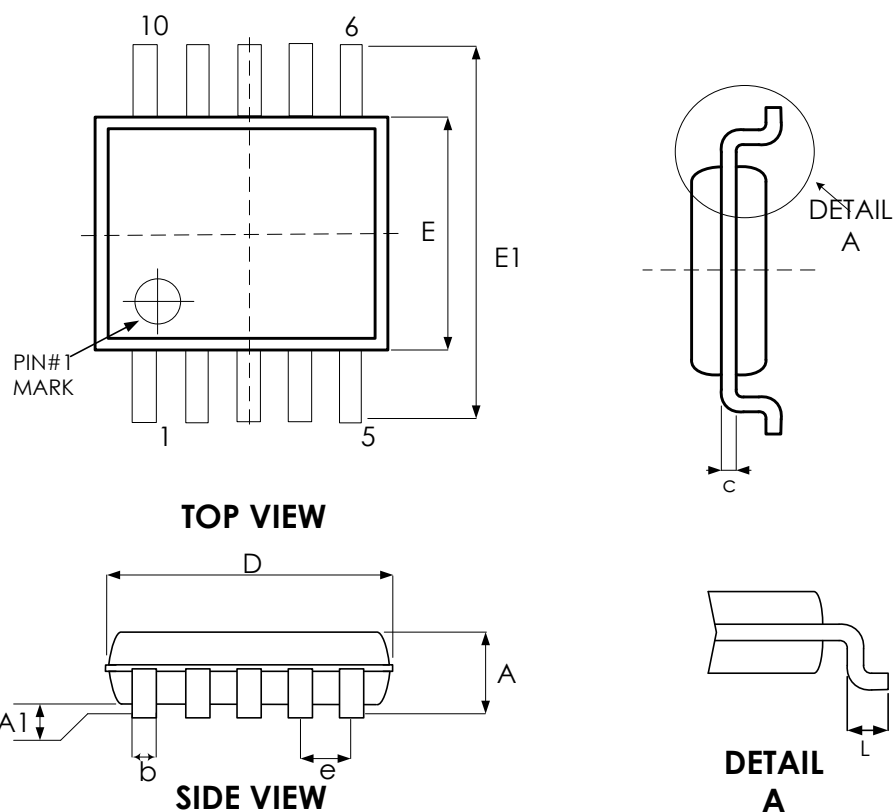


Typical Application Circuit (cont.)

■ Second-Order Active Low-Pass Filter (load support $\geq 600\Omega$ only)



Package Outline Drawing MSOP-10



Symbol	Dimension in mm	
	Min	Max
A	0.81	1.10
A1	0.00	0.15
b	0.17	0.33
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.80	5.00
e	0.50 BSC	
L	0.40	0.80

Revision History

Revision	Date	Description
1.0	2012.09.25	Original
1.1	2012.12	Modify the Pin Description and Package Outline Drawing
1.2	2013.07	Modify ISD max spec from 100uA to 5uA with VDD =5.5V
1.3	2014.01.29	Modify TA from 0~70'C to -40~85'C
1.4	2018.01.03	Update typical application circuit.
1.5	2018.04.13	Update features page 1.

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